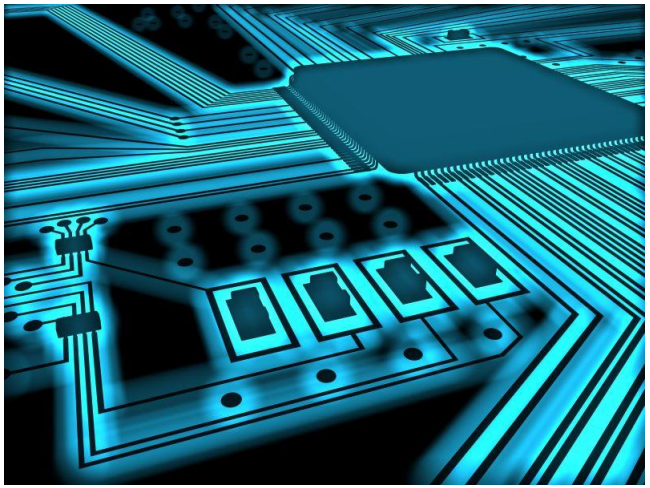


8. Interconnections

Chapter 3, sections 3.3, 3.4

Sections 3.3, 3.4

- Reading:
  - Section 3.3 (pp. 84-85 Interconnection Structures)
  - Section 3.4 (pp. 85-93 Bus Interconnection)
- Good Problems to work: 3.4, 3.5, 3.7, 3.16

Interconnection Structures

- A computer consists of three types of components or modules:
  - processor
  - memory
  - I/O
- Interconnection structure – collection of paths connecting various modules or components

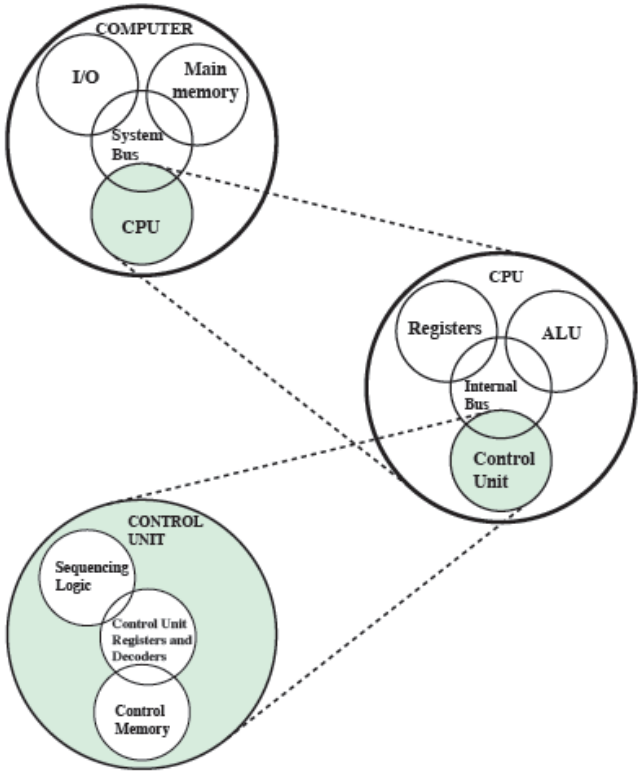
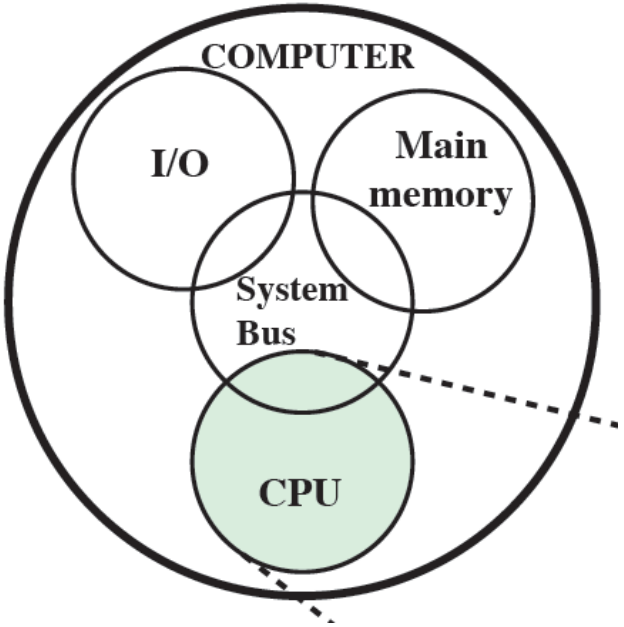


Figure 1.4 A Top-Down View of a Computer

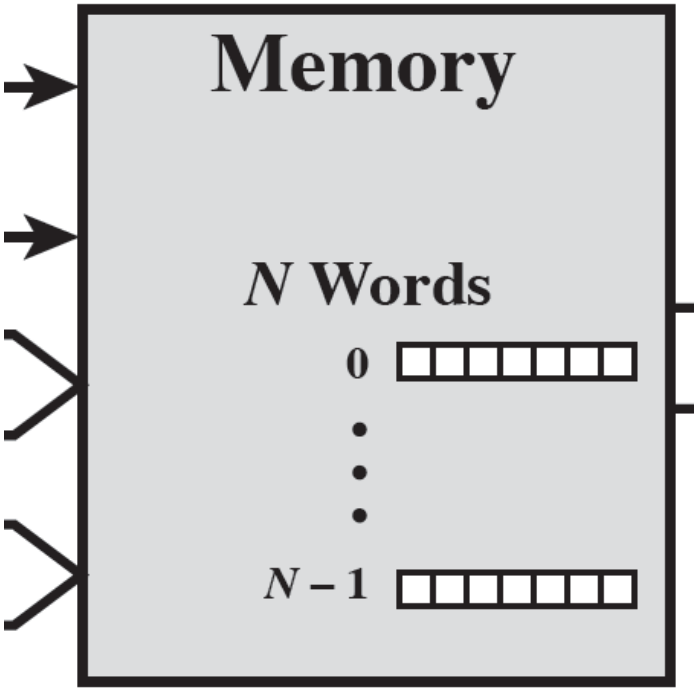
Exchanges

- What exchanges need to happen between the three main components?



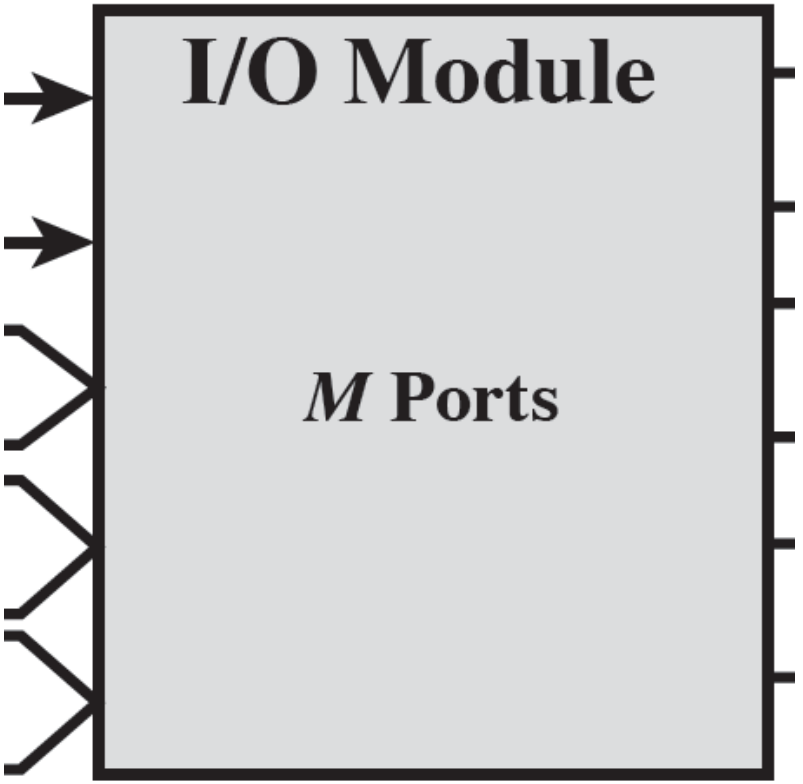
Memory Module

- Memory module consists of N words of equal length



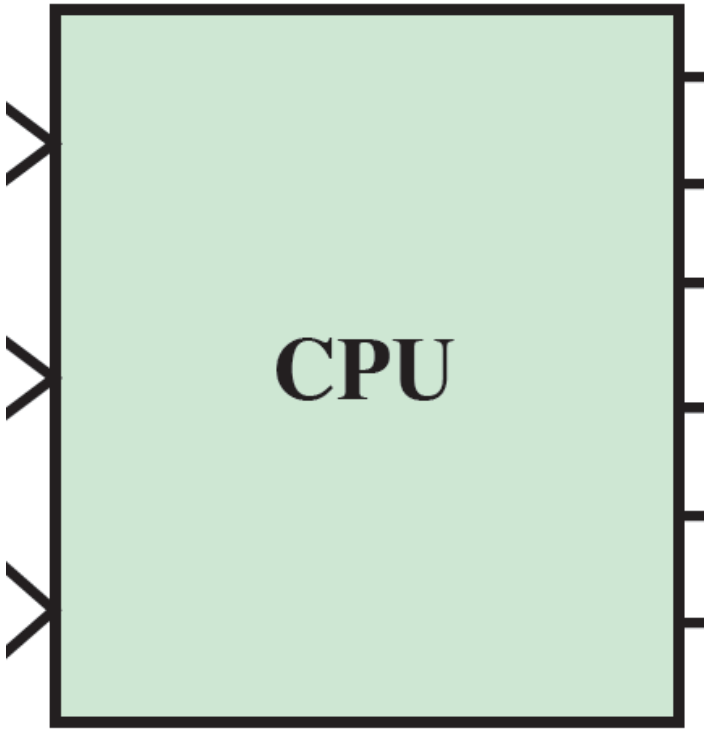
I/O Module

- I/O Module – is similar functionally to memory except:
  - multiple external devices can be controlled through interfaces called ports
  - data can be internal or external
  - I/O can send interrupts



Processor

- The processor
  - reads instructions and data
  - processes data and writes out the results
  - uses control signals to control the overall operation of the system
  - receives interrupt signals



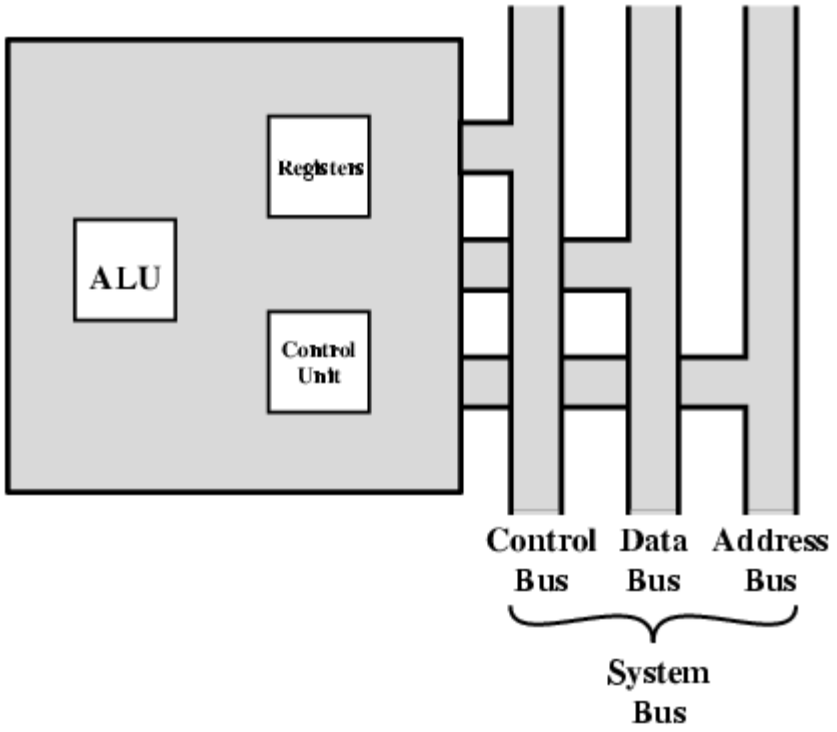
Interconnection Structure

- The interconnection must support the following data exchanges:
  - Memory to Processor
  - Processor to Memory
  - I/O to Processor
  - Processor to I/O
  - I/O to Memory (DMA: Direct Memory Access)
  - Memory to I/O (DMA: Direct Memory Access)

Interconnection Structures

- Bus
- Point-to-point interconnection structures with packetized data transfer

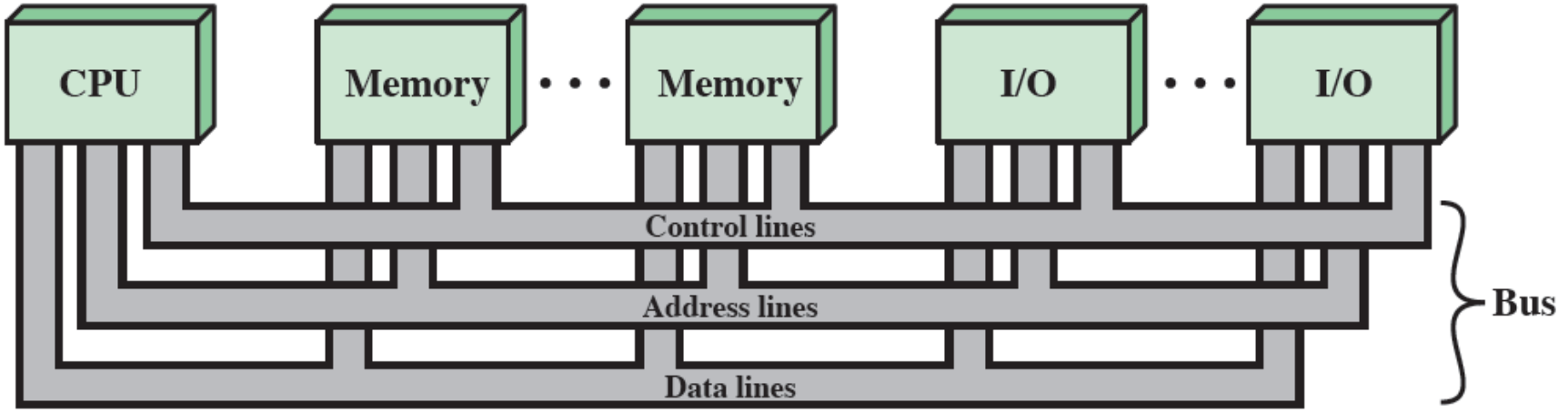
BUS INTERCONNECTION



BUS STRUCTURE

Bus Structure

- Bus – communication pathway connecting two or more devices
- Multiple buses exist in a computer system



Data Lines

- Used for moving data
- Width of data bus is the number of lines
- Width of the data bus affects system performance

Address Lines

- Used for specifying an address either in memory or an I/O
- Higher order bits determine module to access

Control Lines

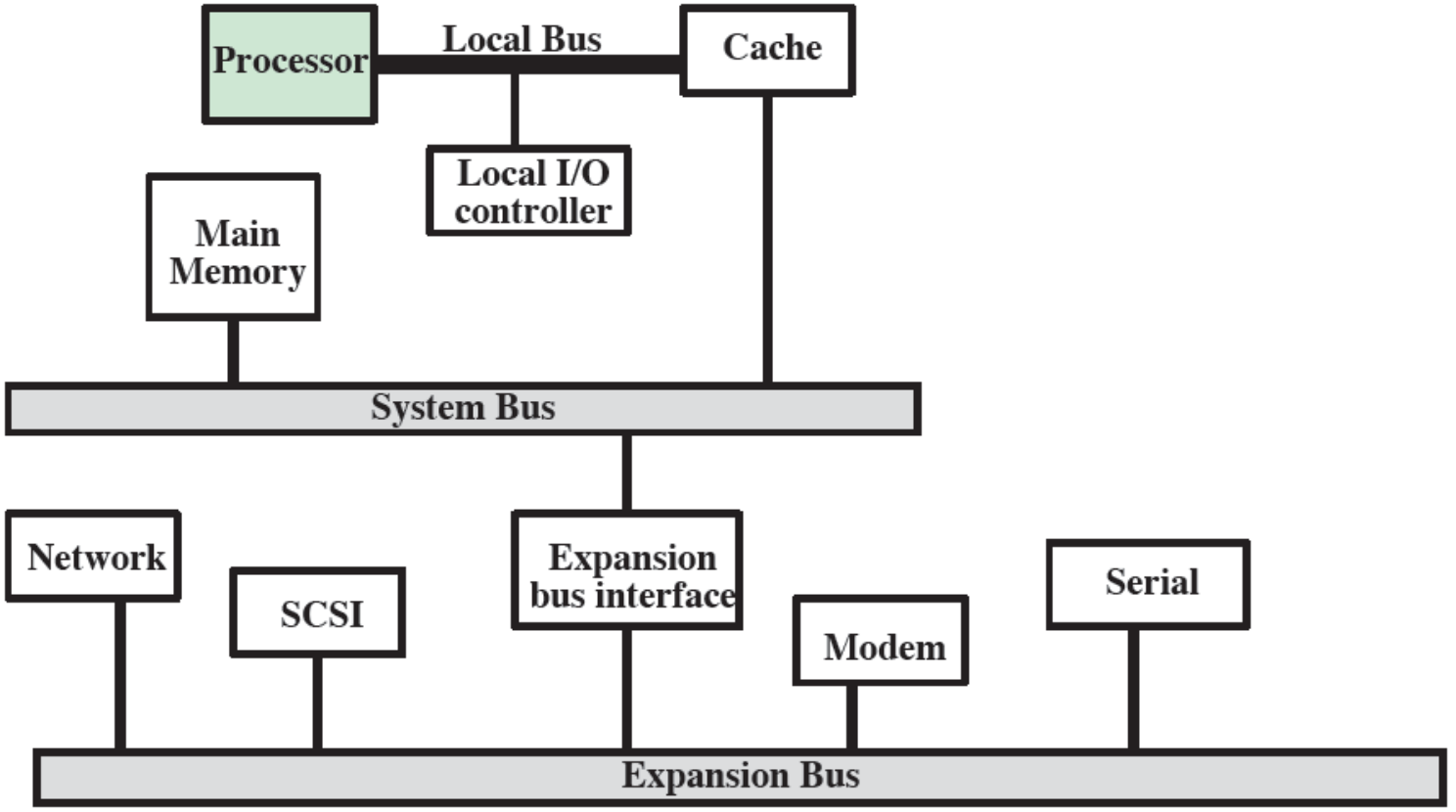
- Memory Write
- Memory Read
- I/O Write
- I/O Read
- Transfer Acknowledge
- Bus Request
- Bus Grant
- Interrupt Request
- Interrupt Acknowledge
- Clock
- Reset

MULTIPLE-BUS HEIRARCHIES

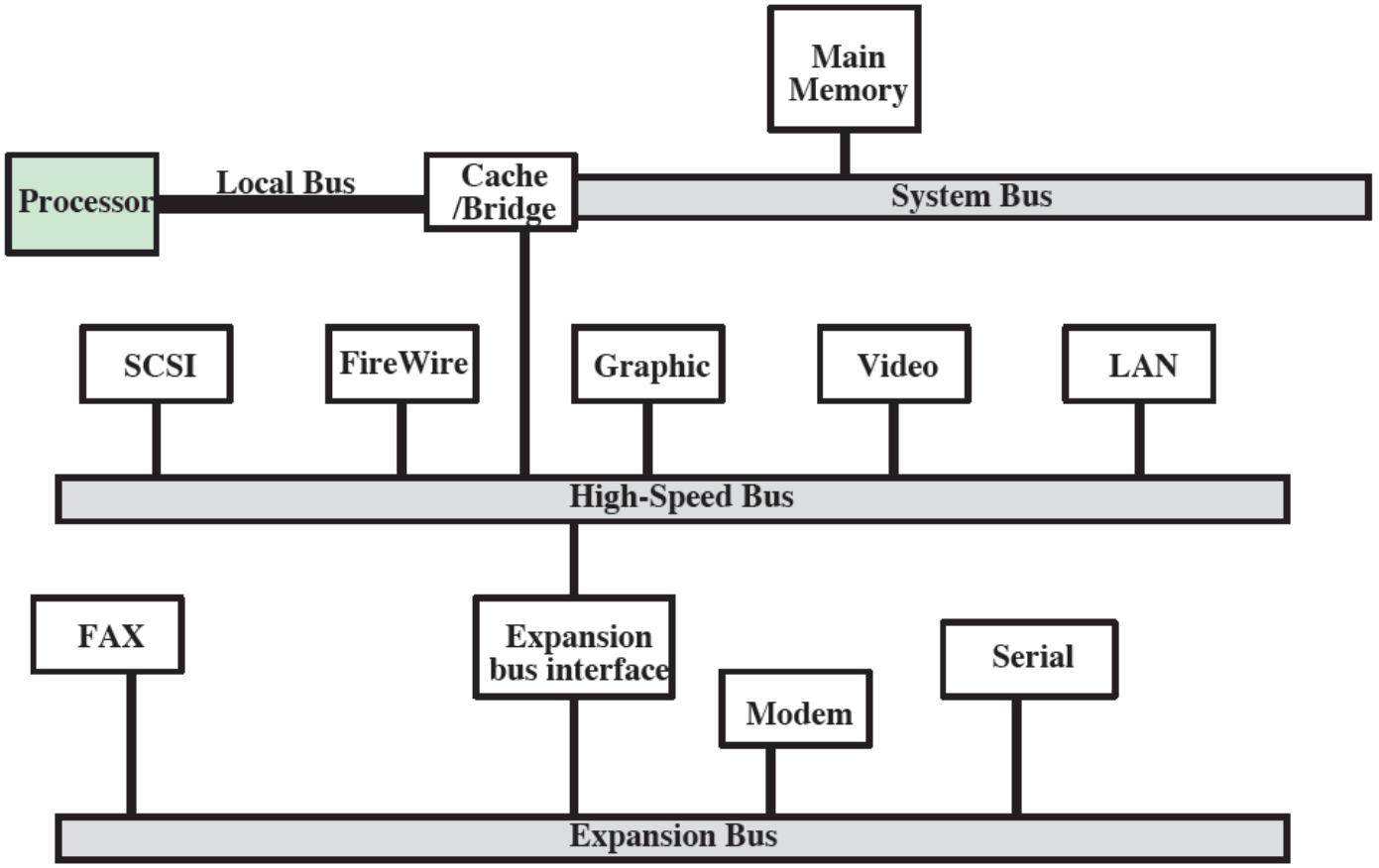
Multiple-Bus Hierarchies

- The more devices connected to a bus, the more likely performance will suffer
  - More devices means greater bus length means greater propagation delay
  - As aggregate data transfer demand approaches the bus capacity, the bus becomes a bottleneck

Traditional Bus Architecture



High-Performance Architecture



ELEMENTS OF BUS DESIGN

Bus Types

- **Dedicated** – assigned to a single function (e.g address bus) or a physical subset of components (e.g. I/O bus connecting I/O modules)
- **Multiplexed** – used for both addresses and data where an address valid control line is needed to determine whether the data is an address or data
- Note: The term multiplexed can also be used as follows: A multiplexed bus can be used to transmit fewer bits of a larger number of bits (e.g. multiplexed 8-bit address bus used to transmit 16-bits of address data)

Method of Arbitration

- **Centralized** – a single hardware device (the bus controller or arbiter) is responsible for allocating time on the bus

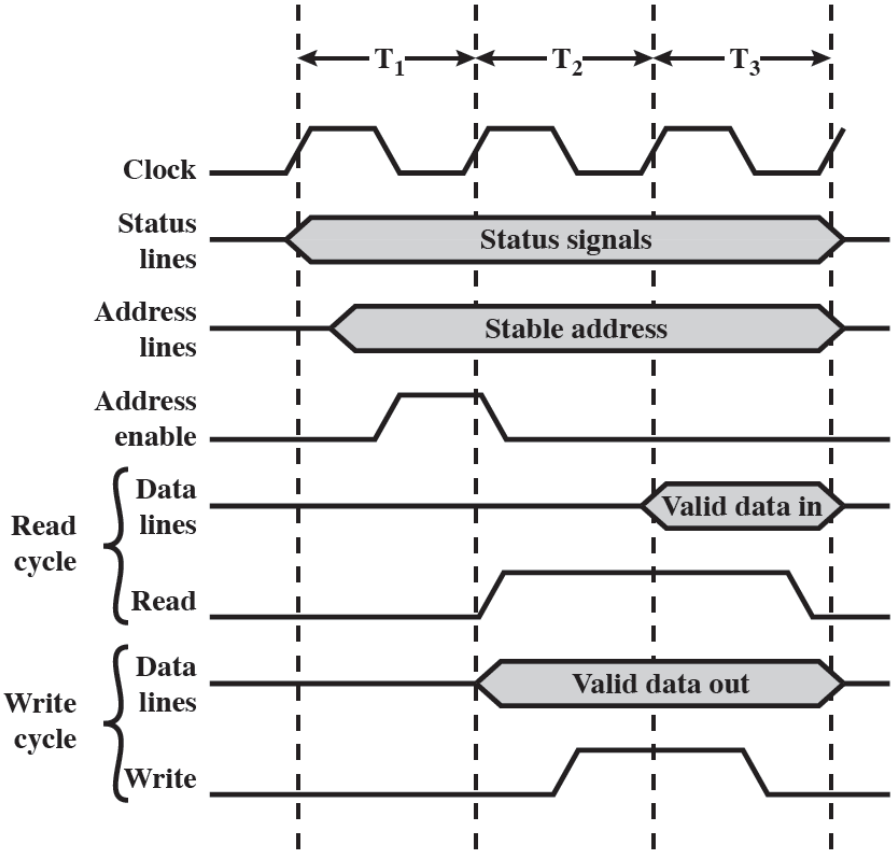
- **Distributed** – has no central controller, instead each module has access control logic where the modules work together to share the bus
  - one module is the master and some other device is the slave

Timing

- **Synchronous** Timing
- **Asynchronous** Timing
- The following slides depict timing diagrams. You can read more about these in appendix N
  - http://www.cs.vassar.edu/~jones/Stallings/N-TimingDIagrams

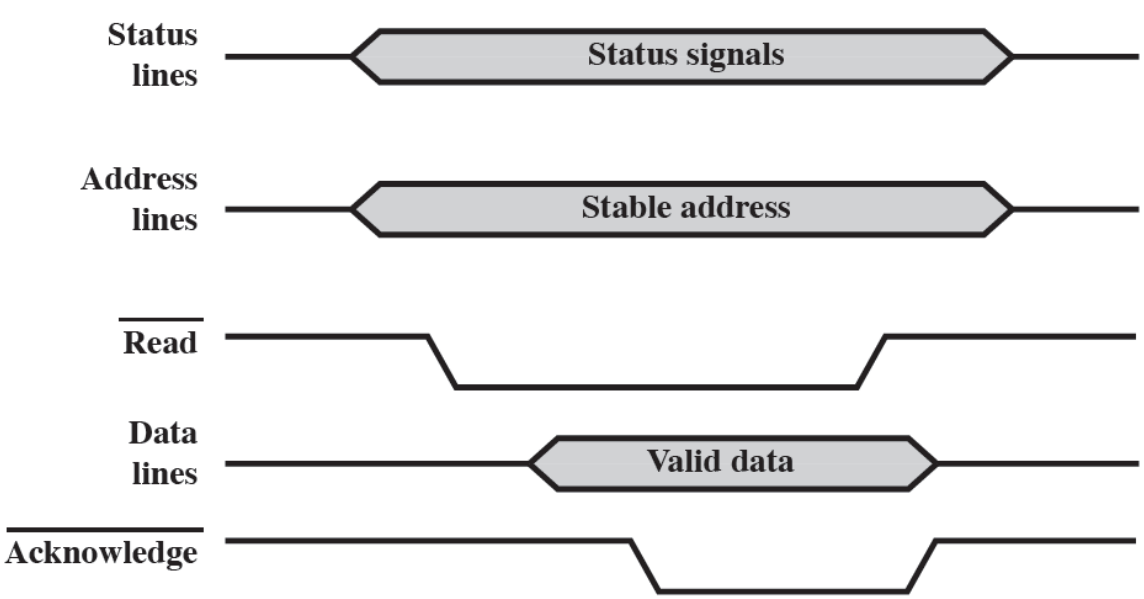
Synchronous Timing

- Synchronous – the clock determines the occurrence of events
- Processor reads from memory and writes to memory



Asynchronous Timing - Read

- Asynchronous – there is no clock
- Processor reads from memory



Asynchronous Timing - Write

- Asynchronous – there is no clock
- Processor writes to memory