# Chapter 5 - Internal Memory

Reading: Section 5.1 on pp. 145-154

Memory Basics

Early memory was made out of doughnut-shaped ferromagnetic loops called cores; thus, today, main memory is still referred to as core memory.

Cache memory is composed of SRAM (static RAM)
- faster
- more expensive
- less dense

Main memory is composed of DRAM (dynamic RAM)
- slower
- less expensive
- more dense

As we've seen, semiconductor memories share the following characteristics:
Two stable states exist to represent a zero or a one
They can be written to (at least once) to set the state
They can be read to sense the state

Most cells look like the following:

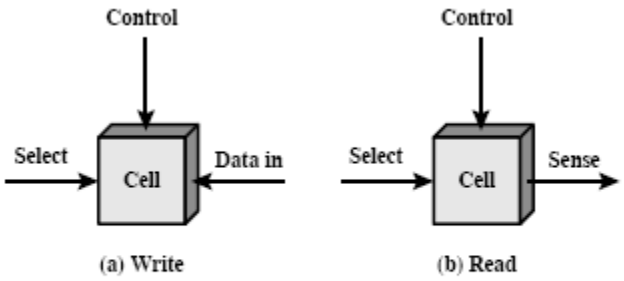



Figure 5.1 Memory Cell Operation

**Table 5.1 Semiconductor Memory Types**

| Memory Type | Category | Erasure | Write Mechanism | Volatility |
|---|---|---|---|---|
| Random-access memory (RAM) | Read-write memory | Electrically, byte-level | Electrically | Volatile |
| Read-only memory (ROM) | Read-only memory | Not possible | Masks | Nonvolatile |
| Programmable ROM (PROM) | | | Electrically | |
| Erasable PROM (EPROM) | Read-mostly memory | UV light, chip-level | | |
| Electrically Erasable PROM (EEPROM) | | Electrically, byte-level | | |
| Flash memory | | Electrically, block-level | | |

Chip Logic

Consider the following diagram:

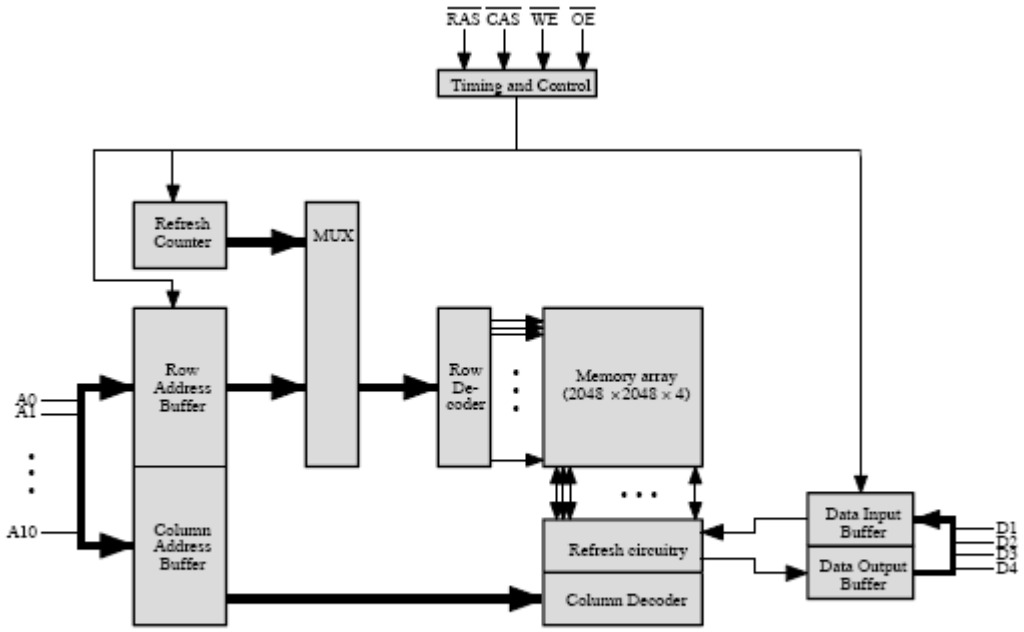


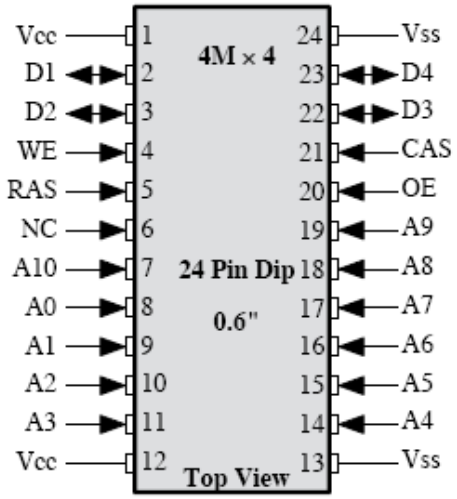

**Figure 5.3 Typical 16 Megabit DRAM (4M × 4)**

Q1: How many bits are read or written at a time?

Q2: How big is the bus used to access a memory location?

Q3: The address bus is multiplexed between the row select and then the column select. What does this mean?

Q4: Multiplexed addressing plus the use of square arrays result in a quadrupling of memory size for each additional pin. How would that apply to the above example? The chip for a 16Mbit DRAM might look like the following:

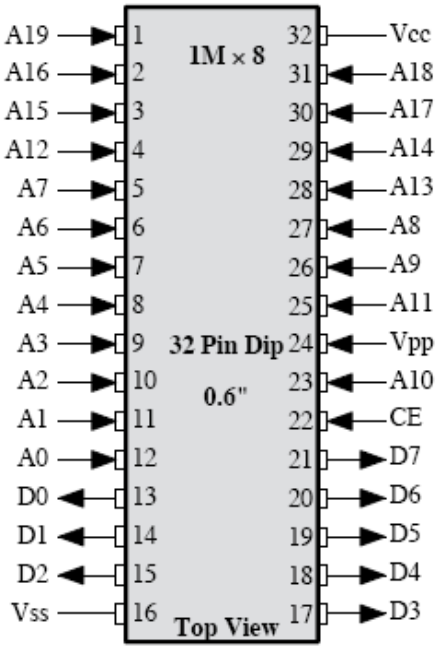



**(b) 16 Mbit DRAM**

"In microelectronics, a **dual in-line package (DIP)**, sometimes called a **DIL** package, is an electronic device package with a rectangular housing and two parallel rows of electrical connecting pins, usually protruding from the longer sides of the package and bent downward. A DIP is usually referred to as a **DIP*n***, where *n* is the total number of pins. For example, a microcircuit package with two rows of seven vertical leads would be a DIP14."

from http://en.wikipedia.org/wiki/Dual_in-line_package

The chip for an 8Mbit EPROM might look like:




(a) 8 Mbit EPROM