CS430 Computer Architecture
Direct Mapping in Caches

Example:

This example uses figure 4.8

$$m \text{ (number of lines in cache)} = 16K = 2^{14}$$
$$i = j \text{ modulo } 2^{14}$$

Address Length is = (s + w) bits

Q#1. What is the size of s?

Q#2. What is the size of w?

Q#3. How many addressable units are there in memory

Q#4. What is the block size in memory?

Q#5. What is the line size in cache?

Q#6. How many blocks are there in memory?

Q#7. How many lines are there in cache?

Q#8. What is the size of the tag?

Let’s draw cache and memory:

Q#9. What is the tag for Block 0? What line will it be transferred to in cache?

Q#10. What is the tag for Block x? What line will it be transferred to in cache?

Q#11. What is the tag for Block y? What line will it be transferred to in cache?

Q#12. What is the tag for Block z? What line will it be transferred to in cache?

Problem 1:

A digital computer has a memory unit of 64K X 16 and a cache memory of 1K byes. The cache uses direct mapping with a block size of four bytes.

Show the address format and indicate how many bits are there in the tag, line, and word fields of the address format?

Problem 2:

The Magiccomputer Corporation manufacturers a machine with a cache that contains four lines. Main memory consists of 16 blocks.

Suppose a program starts out by referencing blocks 0, 3, 4, 9, and 5, in that order. After this series of references is made, which blocks are in the cache, and what are the tags (in binary) if the cache organization is Direct Mapping.

Line	Tag	Block Number
0		
1		
2		
3		