CS430 Computer Architecture
Final Exam Topics

- Chapter 1 – Nothing
- Chapter 2 – Nothing
- Chapter 3 – Computer Function:
  - Instruction cycle
  - Interrupts
  - Bus design: synchronous vs. asynchronous timing
- Chapter 4 – Cache Memory
  - Memory Hierarchy
  - Locality of Reference
  - Cache Design
    - Direct Mapping
    - Associative Mapping
    - Set-Associative Mapping
    - Replacement Algorithms
- Chapter 5 – Internal Memory: section 5.1
  - Difference between DRAM and SRAM
- Chapter 6 – Nothing
- Chapter 7 – Nothing
- Chapter 8 – Nothing
- Chapter 9 – Computer Arithmetic:
  - Sign-magnitude
  - One's complement
  - Two's complement
  - Integer addition and subtraction
  - IEEE floating point representation
- Chapter 10 – Machine Instructions:
  - Advantages and disadvantages of the possible number of addresses
  - Packed decimal: what is it?
  - Endianness
  - Difference between arithmetic shift and regular shift
  - Branching and stack frames
- Chapter 11 – Addressing modes
  - What is an effective address?
  - Describe any of the addressing modes.
- Chapter 12 – Processor Structure and Function
  - Registers
  - Segment pointer and offset
  - Control and status registers
  - Instruction cycle
  - Speedup
  - Instruction pipelining
  - Pipeline hazards

    - Loop buffer
    - Branch prediction
    - Interrupt Processing: interrupt vector table and interrupt handling
- Chapter 13 – RISC
    - Register windows
    - Compiler based register organization – graph coloring
    - Section 13.5: RISC pipelining
    - Describe x number of differences between RISC and CISC
- Chapter 14 – Instruction Level Parallelism: sections 14.1 and 14.2 that Maggie covered
    - You need to be able to describe what superpipelined and superscalar mean
    - You need to be able to describe the 5 limitations of parallelism
- Chapter 15 – I-64: the sections that PJ covered
    - What was the motivation for IA-64?
    - What's the difference between prediction and speculative loading?
- Chapter 16 – Micro-Operations: sections 16.1 and 16.2 that Perry covered
    - What are micro-operations? Give examples of the operations during the fetch, indirect or interrupt cycles.
    - Describe the two tasks of the control unit?
- Chapter 17 – Microinstructions: sections 17.1 and 17.2
    - What is a microprogrammed control unit and is it used by CISC or RISC systems?
    - What is the difference between horizontal and vertical microinstructions?
- Chapter 18 – Parallel Processing: everything covered by Donald and Erik
    - You need to understand how cache coherency works for the MESI protocol.
    - You need to be able to briefly describe clusters, NUMA, and Vector computing.

Random question: here's a pipeline:

```
--1--2--3--4--5--6--7--8--9--0--1--2--3--4--5
 IF ID EX  M WB
    IF ID EX  M WB
       IF ID EX  M WB
and so on
```

Assume the execution of a nonpipelined machine with 5 stages (IF,ID,EX,M,WB) and execution lengths of 40ns, 50ns, 40ns, 40ns, and 40ns. If pipelining the machine costs an extra 5ns of overhead, what is the speedup of the pipelined machine. Think hard on this one, the answer is not obvious.