CS 430 Problem Set #3

Date assigned: Friday, September 26, 2008
Date due: Wednesday, October 8, 2008
Points: 40

1. (5 pts) Consider a synchronous bus that has a 50 MHz clock. The bus is 64-bits wide and has multiplexed data and address lines. A bus read transaction to read a single 64-bit word from memory takes a total of four clock cycles as follows: (a) 1 to transmit the address (b) 2 delay cycles for the memory to work (c) and on the fourth cycle, the word is transmitted. In millions of bytes per second (MB/s), state what the bandwidth if this bus is for single-word transfers.

2. (5 pts) Consider the bus from question 1) is connected to a cache with 32-byte cache lines. A read-multiple transaction would: (a) transmit the cache line address during the first cycle (b) delay for 2 cycles for the memory to work (c) transmit one word from memory per cycle thereafter. What is the bandwidth of this bus for cache line fills?

3. (15 pts) Assume a 16-word cache that is two-way set associative with 2-word cache lines. Further, the replacement policy is LRU (least recently used). Show the cache after the following sequence of address references where all references are instruction or data fetches and no store operations.

   62
   63
   64
   98
   65
   99
   66
   99
   67
   68
   69
   6a
   63
   64
   6C
   65
   6D
   66
   6D
   67
   68
   69

4. (10 pts) Work problem 4.5 on p. 133. The block diagram is to resemble the figure on p. 122. The only address that is mapped is ABCDE8F8.

5. (13 pts) Work problem 4.12 on p. 134.

You may submit this assignment in one of two way: (1) a Google document shared with ShereenKhoja@gmail.com, (2) a Word document attached to an email sent to ShereenKhoja@gmail.com. Do not submit a hard copy.