CS430 Computer Architecture

## Spring 2015

Chapter 3

- Reading:
  - Section 3.3 (pp. 84-85 Interconnection Structures)
  - Section 3.4 (pp. 85-93 Bus Interconnection)

- Good Problems to work: 3.4, 3.5, 3.7, 3.16

Interconnection Structures

- A computer consists of three types of components or modules:

    1. processor

    2. memory

    3. I/O

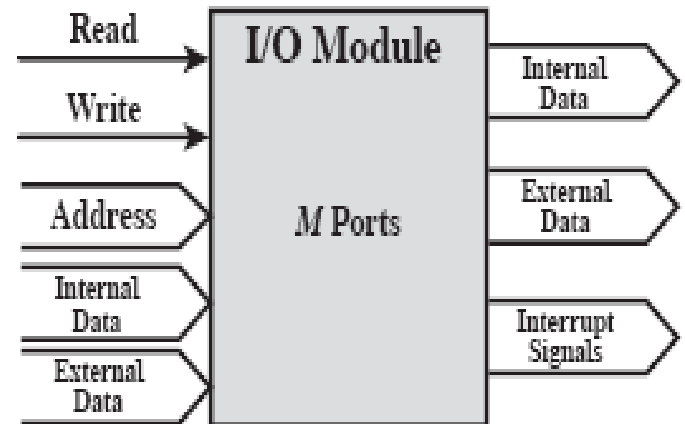- interconnection structure – collection of paths connecting various modules or components

Memory Module

- Memory module consists of N words of equal length
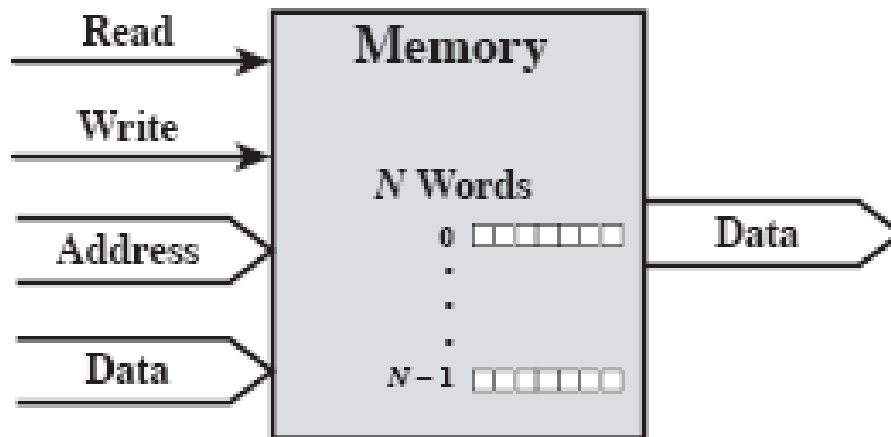
I/O Module

- I/O Module – is similar functionally to memory except:

  1. multiple external devices can be controlled through interfaces called ports

  2. data can be internal or externa

  3. I/O can send interrupts

Processor

- The processor

   1. reads instructions and data

   2. processes data and writes out the results

   3. uses control signals to control the overall operation of the system

   4. receives interrupt signals
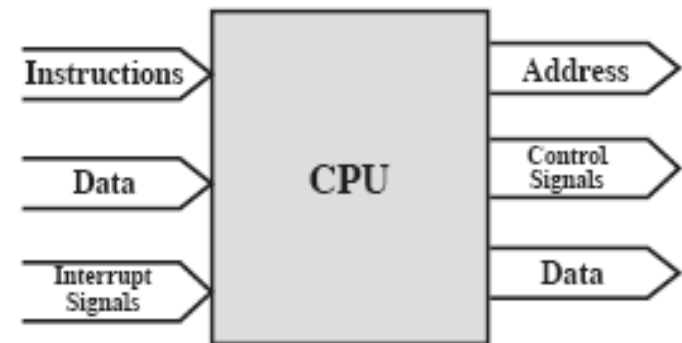
Interconnection Structure

- The interconnection must support the following data exchanges:

  1. Memory to Processor
  2. Processor to Memory
  3. I/O to Processor
  4. Processor to I/O
  5. I/O to Memory
  6. Memory to I/O

- Note: 5. and 6. can use DMA (Direct Memory Access) and avoid processor intervention

Bus Structure

- bus – communication pathway connecting two or more devices

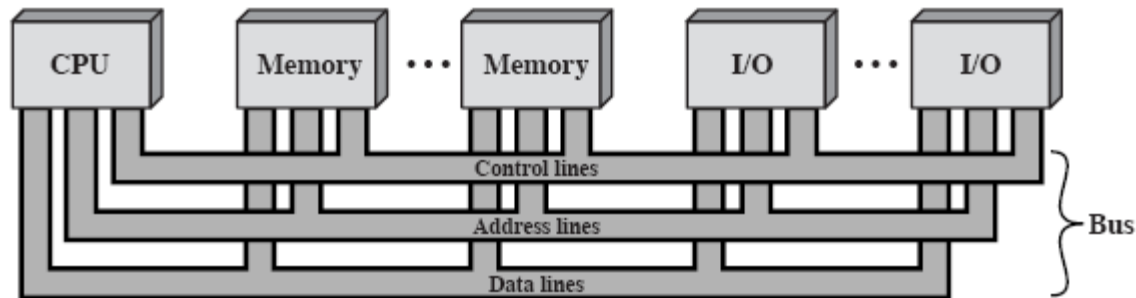- Multiple buses exist in a computer system


Figure 3.16 Bus Interconnection Scheme

Control Lines

- Memory Write
- Memory Read
- I/O Write
- I/O Read
- Transfer Acknowledge
- Bus Request
- Bus Grant
- Interrupt Request
- Interrupt Acknowledge
- Clock
- Reset

Multiple-Bus Hierarchies

- The more devices connected to a bus, the more likely performance will suffer

  1. More devices means greater bus length means greater propagation delay

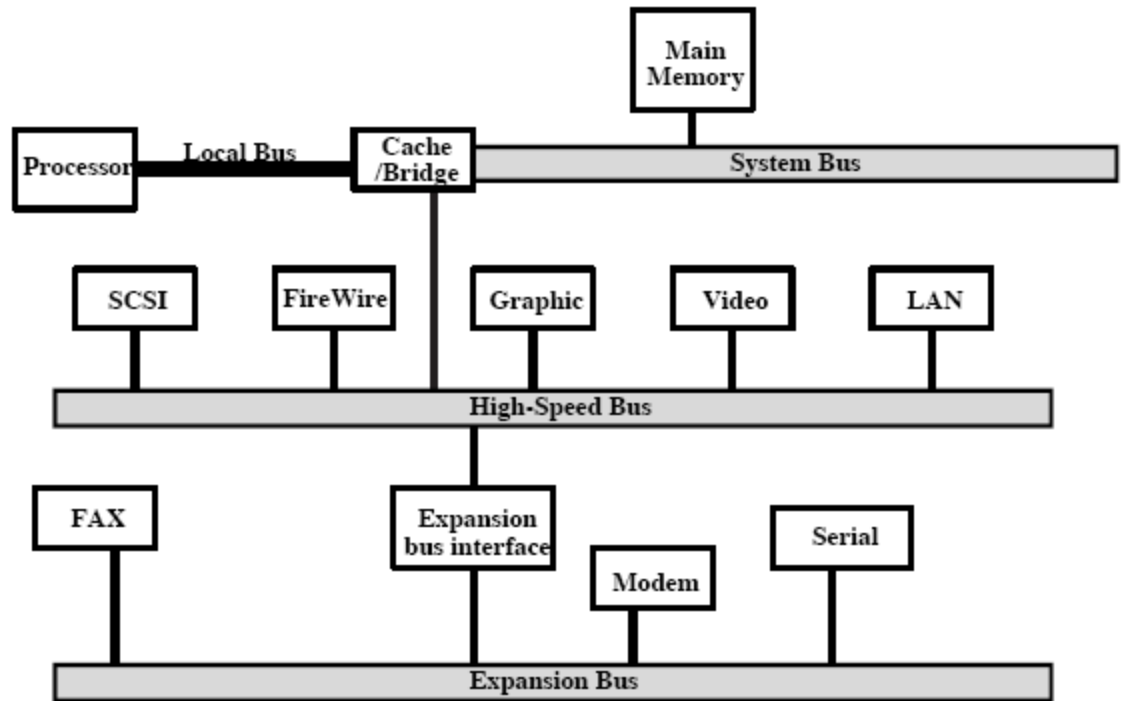 2. As aggregate data transfer demand approaches the bus capacity the bus becomes a bottleneck

Traditional Bus Architecture
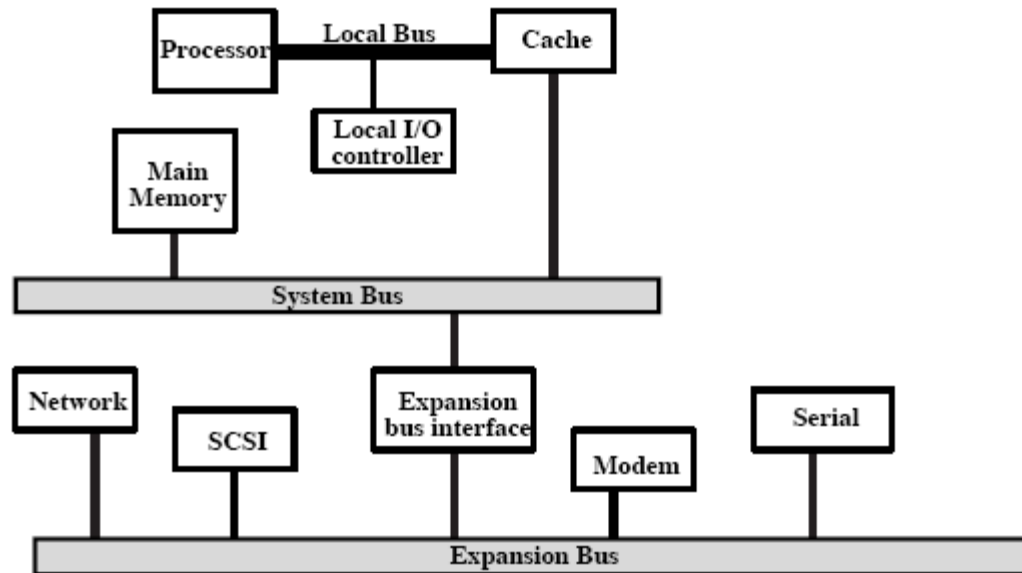
(a) Traditional Bus Architecture

High-Performance Architecture

- As I/O devices have achieved higher performance, the traditional architecture does not deliver optimum performance

(b) High-Performance Architecture

Elements of Bus Design

- ## Bus Types

  - ➢ dedicated – assigned to a single function (e.g address bus) or a physical subset of components (e.g. I/O bus connecting I/O modules)

  - ➢ multiplexed – used for both addresses and data where an address valid control line is needed to determine whether the data is an address or data

Method of Arbitration

- centralized – a single hardware device (the bus controller or arbiter) is responsible for allocating time on the bus

- distributed – has no central controller, instead each module has access control logic where the modules work together to share the bus

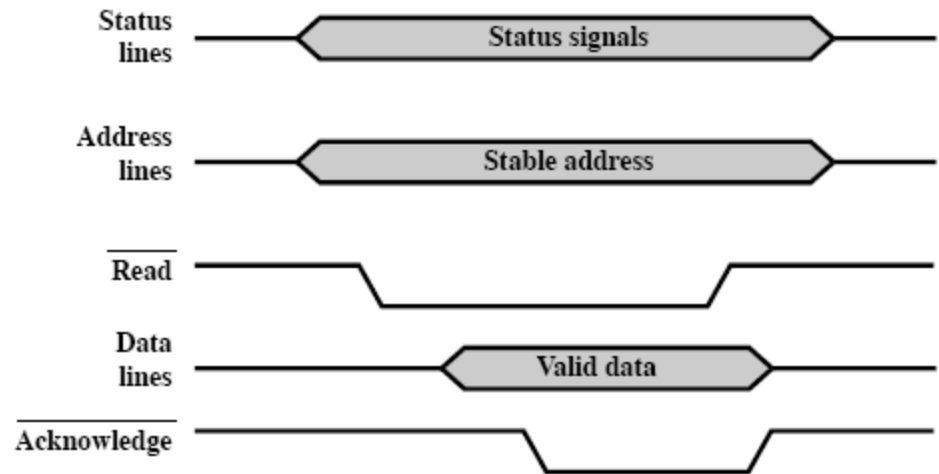 ➢ one module is the master and some other device is the slave

Synchronous Timing

- synchronous – the clock determines the occurrence of events

- processor reads from memory and writes to memory

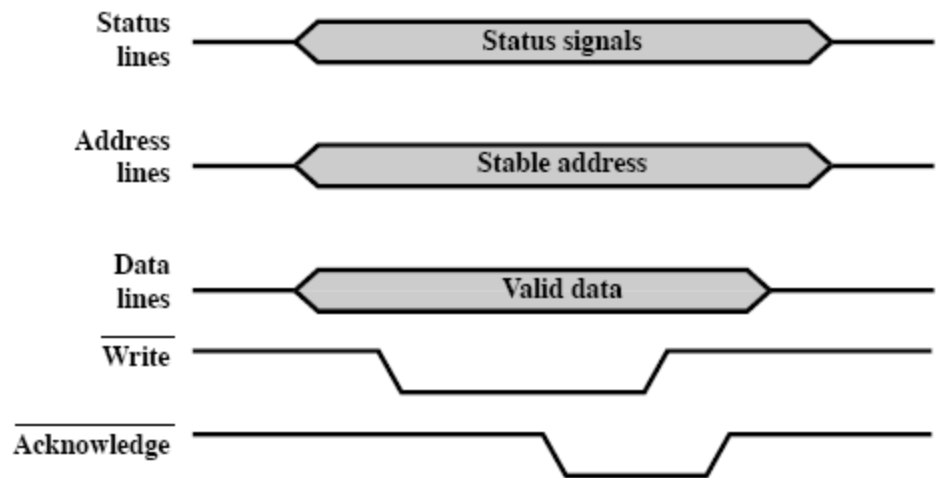- Explain
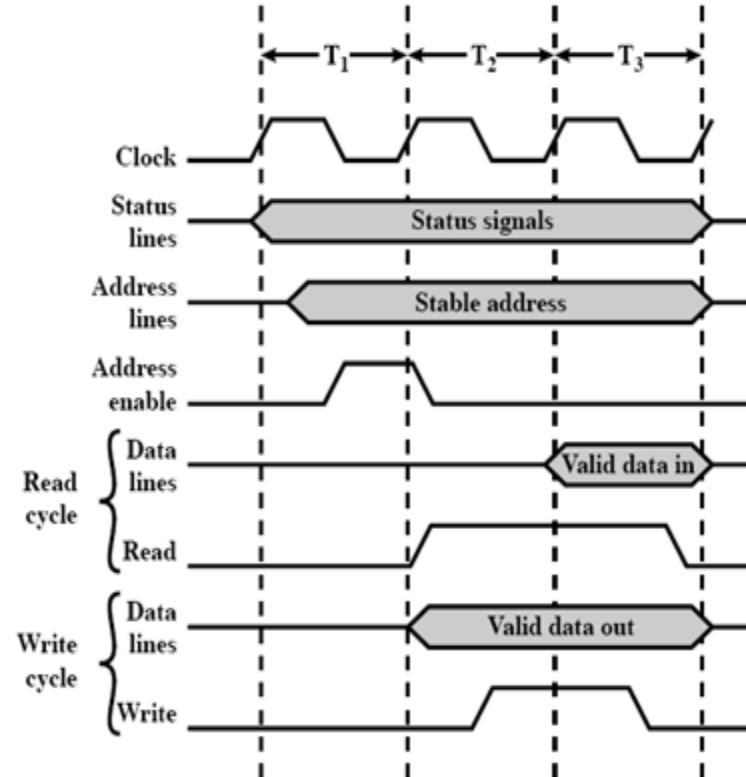
Asynchronous Timing - Read

- asynchronous – there is no clock

- processor reads from memory

- Explain

(a) System bus read cycle

Asynchronous Timing - Write

- asynchronous – there is no clock

- processor writes to memory

- Explain

(b) System bus write cycle