CS430 Computer Architecture
Final Exam Topics

- Chapter 1 – Introduction
  - Computer Architecture
  - Computer Organization
- Chapter 2 – Computer Evolution & Performance
  - Performance Assessment
  - Speedup
  - %faster
  - fraction enhanced
  - digital logic
- Chapter 3 – Computer Function & Interconnection:
  - Instruction cycle
  - Interrupts
  - Bus design: synchronous vs. asynchronous timing
- Chapter 4 – Cache Memory
  - Memory Hierarchy
  - Locality of Reference
  - Cache Design
    - Direct Mapping
    - Associative Mapping
    - Set-Associative Mapping
    - Replacement Algorithms
- Chapter 5 - Nothing
- Chapter 6 – Nothing
- Chapter 7 – Nothing
- Chapter 8 – Nothing
- Chapter 9 - Number Systems
  - Binary
  - Decimal
  - Hex
  - Converting between bases
- Chapter 10 – Computer Arithmetic:
  - Sign-magnitude
  - One's complement
  - Two's complement
  - Integer addition and subtraction
  - IEEE floating-point representation
  - Arithmetic Overflow (signed/unsigned)
- Chapter 11 - Digital Logic
  - Boolean Algebra
  - POS & SOP
  - Gates
  - Combinational Circuits

    - Multiplexer
    - Decoder
    - K maps
- Chapter 12 – Instruction Sets:
    - Advantages and disadvantages of the possible number of addresses
    - Packed decimal: what is it?
    - Endianness
    - Branching and stack frames
- Chapter 13 – Addressing modes and formats
    - What is an effective address?
    - Segmented Memory & the x86
    - Describe any of the addressing modes.
    - Assembly language
- Chapter 14 – Processor Structure and Function
    - Registers (user-visible, control & status)
    - Condition Codes
    - signed versus unsigned instructions
    - Segment pointer and offset
    - Control and status registers
    - Instruction cycle
    - Speedup
    - Instruction pipelining
    - Pipeline hazards (structural, control, data)
    - Loop buffer
    - Branch prediction
    - Dealing with branch hazards
    - Interrupt Processing: interrupt vector table and interrupt handling
- Chapter 15 – RISC
    - RISC versus CISC
    - MIPS Processor (non-pipelined)
    - MIPS 5-stage pipeline
    - RISC pipelining
    - data forwarding using special registers between pipeline stages
    - Describe x number of differences between RISC and CISC
    - MIPS assembly