CS430
Problem Set #2

Date assigned: Monday, September 17, 2012
Date due: Monday, September 24, 2012
Points: 50

1) (10 pts) Work problem 3.3 on p. 109

2) (5 pts) Consider a synchronous bus that has a 50 MHz clock. The bus is 64-bits wide and has multiplexed data and address lines. A bus read transaction to read a single 64-bit word from memory takes a total of four clock cycles as follows: (a) 1 to transmit the address (b) 2 delay cycles for the memory to work (c) and on the fourth cycle, the word is transmitted. In millions of bytes per second (MB/s), state what the bandwidth is if this bus is for single-word transfers.

3) (10 pts) Work problem 3.5 on p. 109

4) (5 pts) Assume that an 8KB L1 cache contains 8 byte lines and has an access time of .01 μs and a 64 KB L2 cache contains 8 byte lines and has an access time of .1 μs. If 95% of the memory accesses are found in the L1 cache, what is the average access time to access a word from the two levels of cache?

5) (6 pts) Work problem 4.3 on p. 147. Do a. only.

6) (14 pts) Work problem 4.8 on p. 148

Note1: Please make sure your problem sets are typed, answered in order, and stapled together.

Note2: A hard copy of your Problem Set Solution is due on the instructor's desk by 11:45am on the day the assignment is due. Also, place a copy of this solution 02PUNetID.doc in the CS430 Drop Box by 11:45am on the day in which the assignment is due.

Note3: I don't mind you talking about particular problems at a very high level (not a specific solution level) and even lending resources of where more information can be found. Further, all of your solutions are to be original and in your own words. If you have any questions, let me know.