CS480

Compilers
Chapter 9
Code Generation in Real Life

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Machines/Assembly Languages

• Register Machines

x = 1 + y;

• Stack Machines

• Our Interpreter

Memory
Heap
Stack
Register
RAM
Cache
Code Generation Considerations

• Instruction Selection
  – correctness
  – speed

• Register Allocation

• Instruction Ordering
Code Analysis

• Basic Blocks

• Flow Graphs
BB Transformations

• Common sub expression elimination

• dead-code elimination

• renaming of temporary variables

• reorder adjacent statements
Next-Use