Resources

https://pdos.csail.mit.edu/6.828/2005/readings/i386/s05_01.htm

http://www.cs.columbia.edu/~junfeng/10sp-w4118/lectures/l23-vm-linux.pdf

http://linux.linti.unlp.edu.ar/images/5/50/Ulk3-cap2.pdf

Segmentation

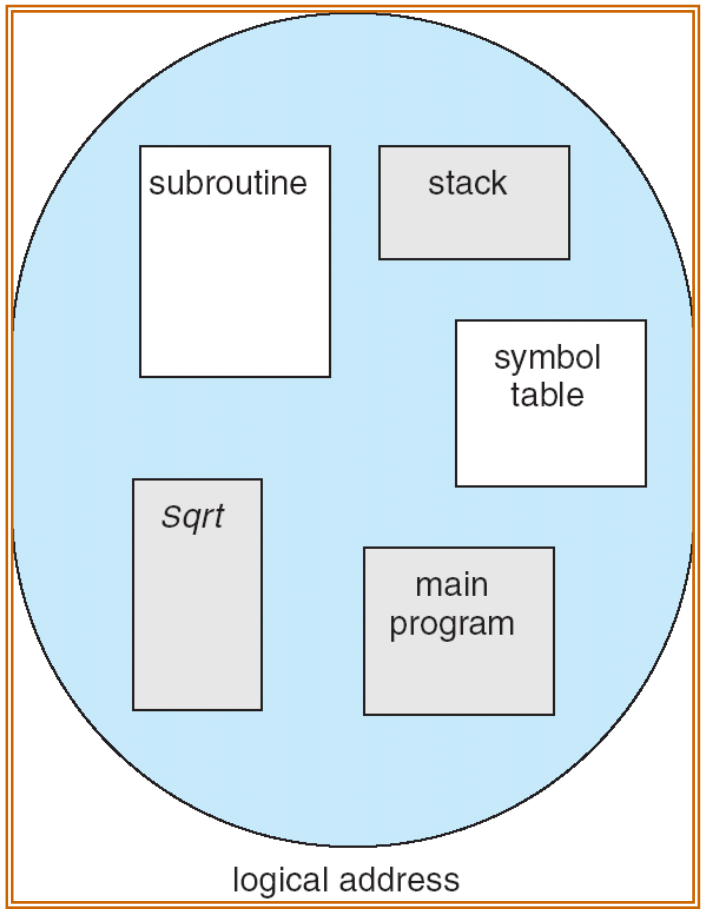
- Address segments of memory
  - Segment identifier + offset
- Intel 8086
  - 16 bits segment register + 16 bit offset
  - 20 pins to access memory (real mode)
  - CPU -> segmentation unit -> paging unit -> physical memory
- 286
  - Protected mode: 24 bits of address, segment register indexes into table of 24 bit addresses (tables: GDT, LDT, registers: GDTR, LDTR)
- 386: paging added, 32 bits of address

Registers

- CS: code – Linux uses part of the cs register to track kernel/user mode
- DS: data
- SS: stack
- ES: extra
- FS, GS: unspecified, introduced with 386 processor

- Implicitly used by instructions

User's View of a Program



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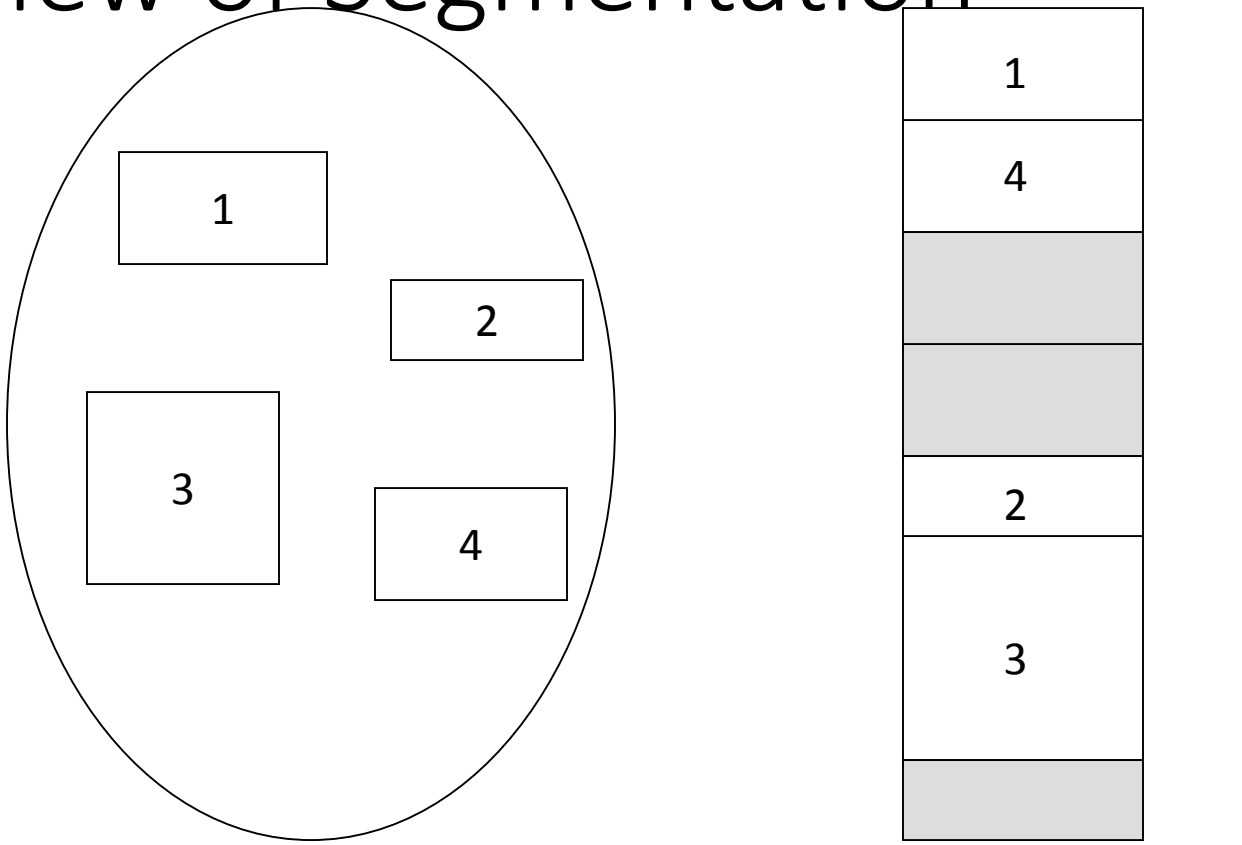
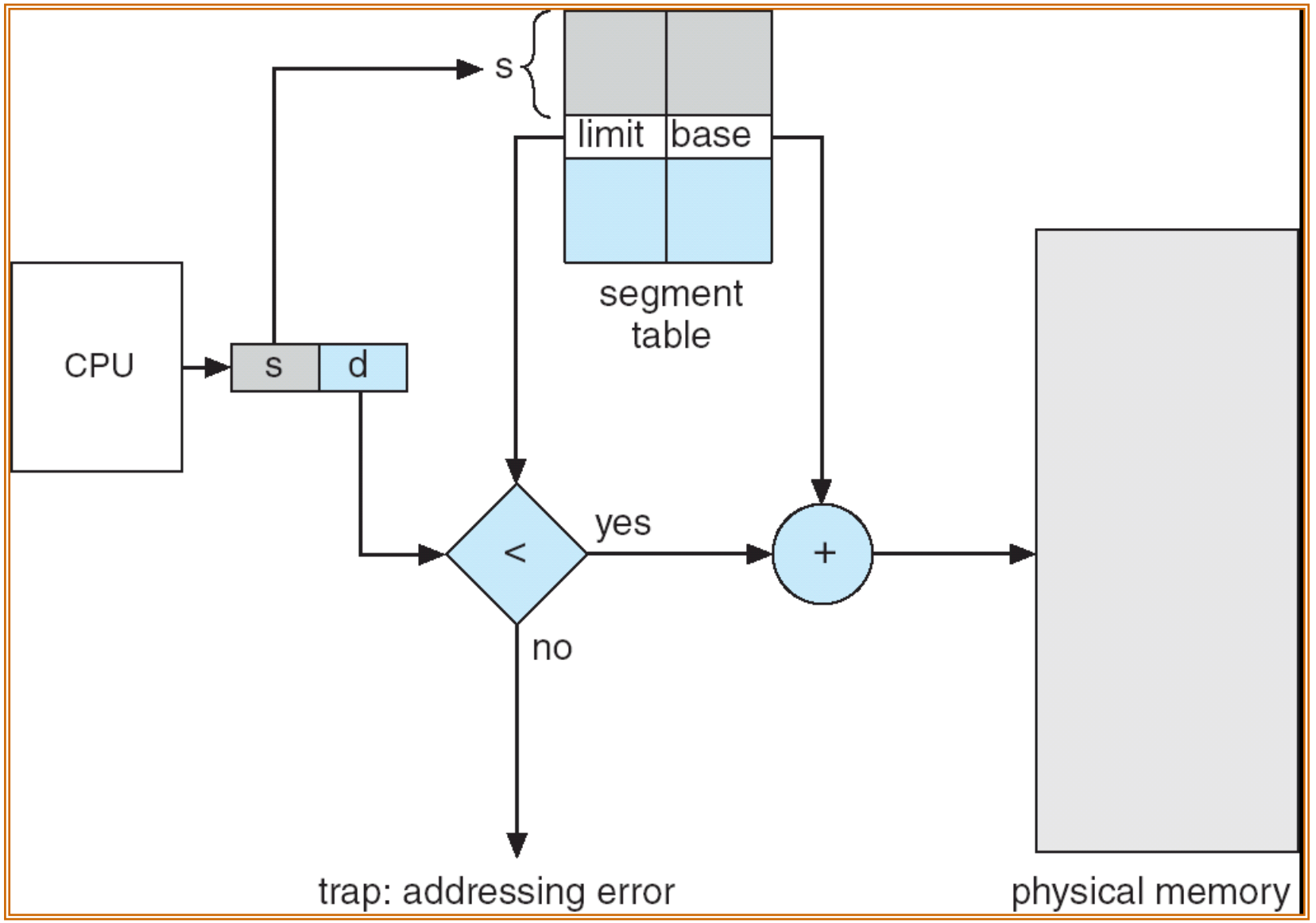
Logical View of Segmentation



Segmentation Hardware



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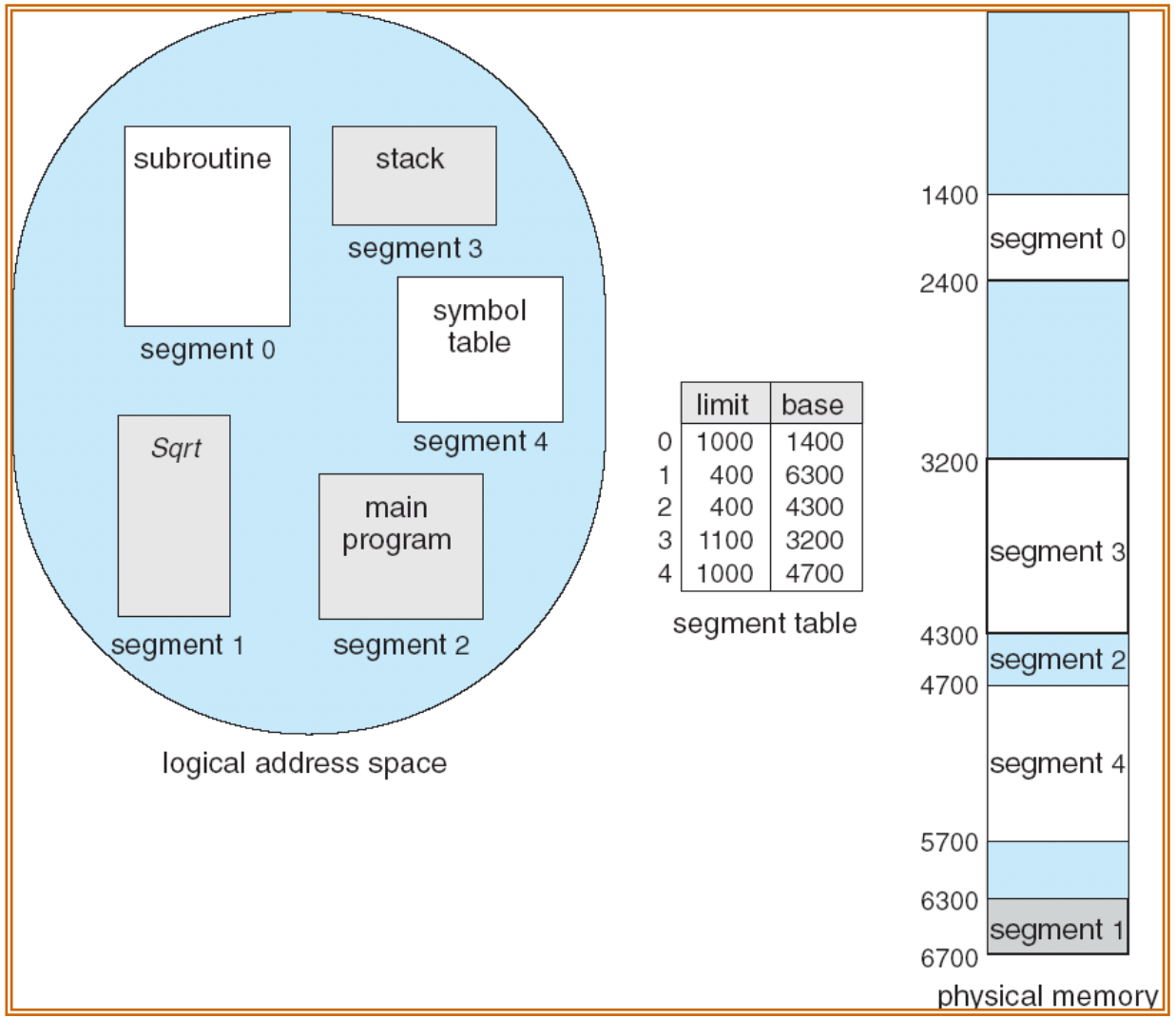
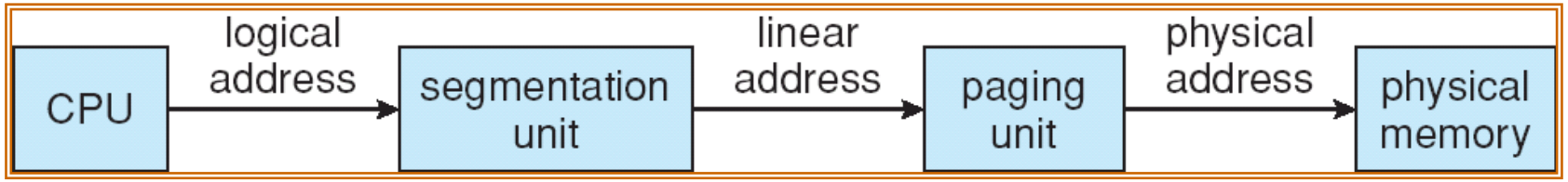
Example of Segmentation



Example: The Intel Pentium

- Supports both segmentation and segmentation with paging
- CPU generates logical address
  - Given to segmentation unit
    - Which produces linear addresses
  - Linear address given to paging unit
    - Which generates physical address in main memory
    - Paging units form equivalent of MMU

Logical to Physical Address Translation in Pentium



page number		page offset
p_1	p_2	d
10	10	12

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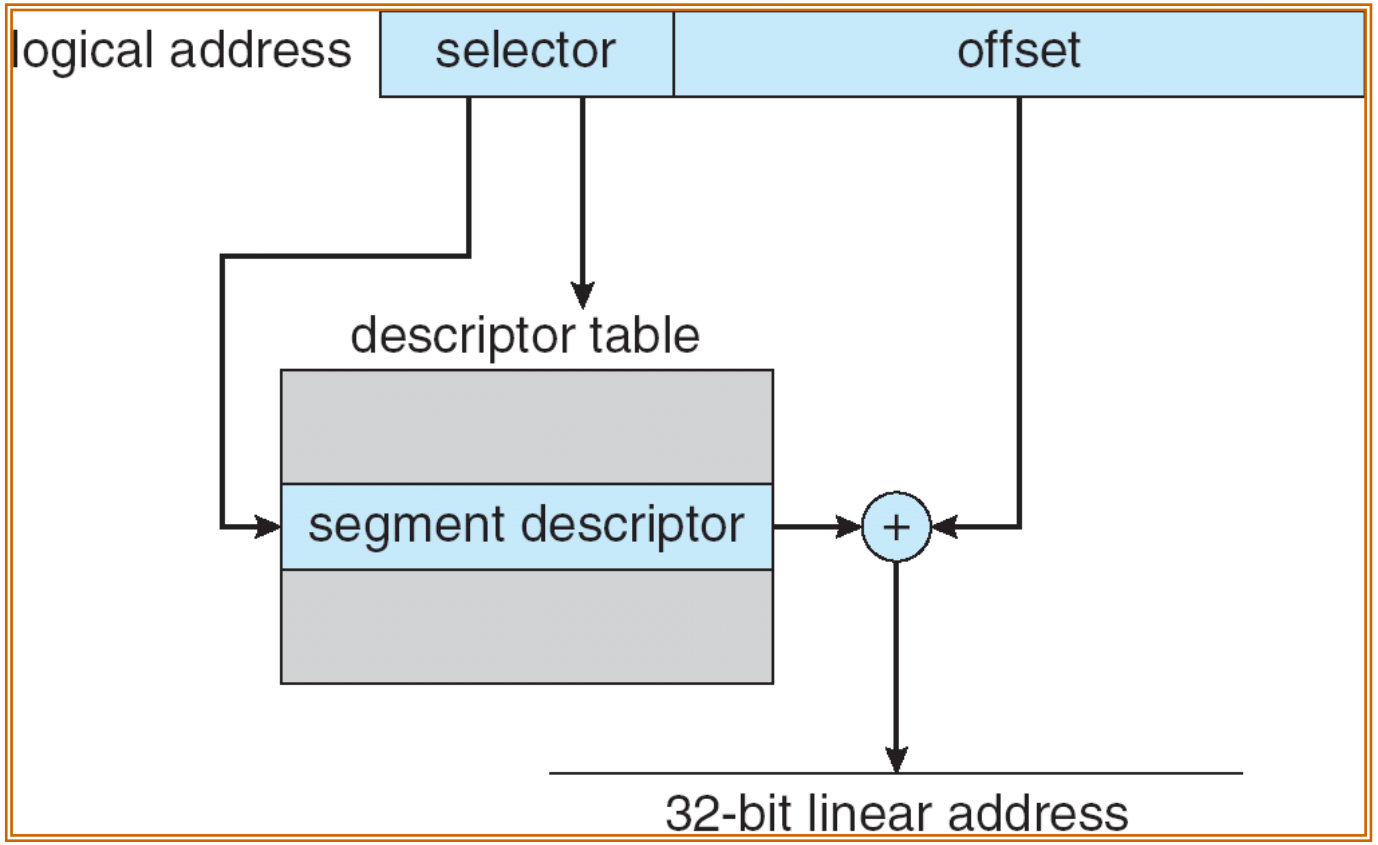
Intel Pentium Segmentation



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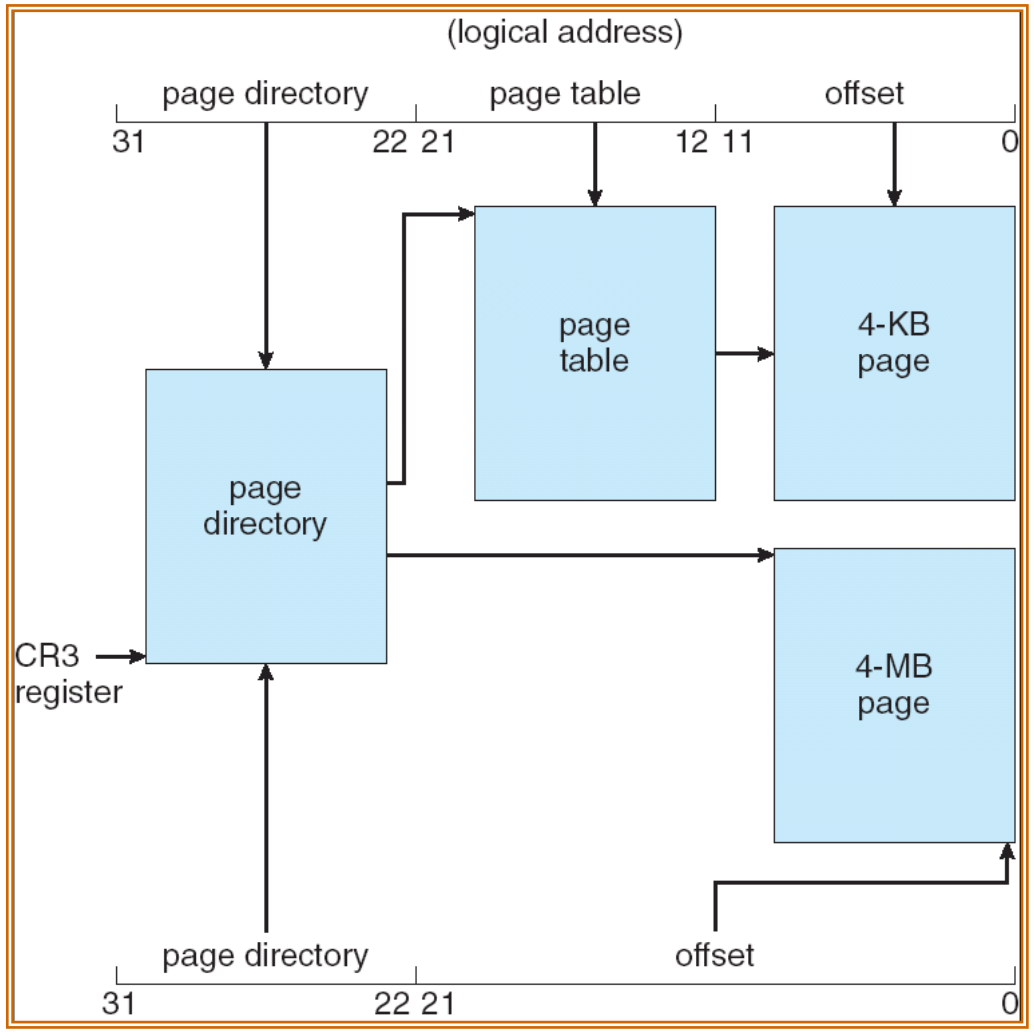
Pentium Paging Architecture



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Linear Address in Linux (non-x86_64)

Broken into four parts:

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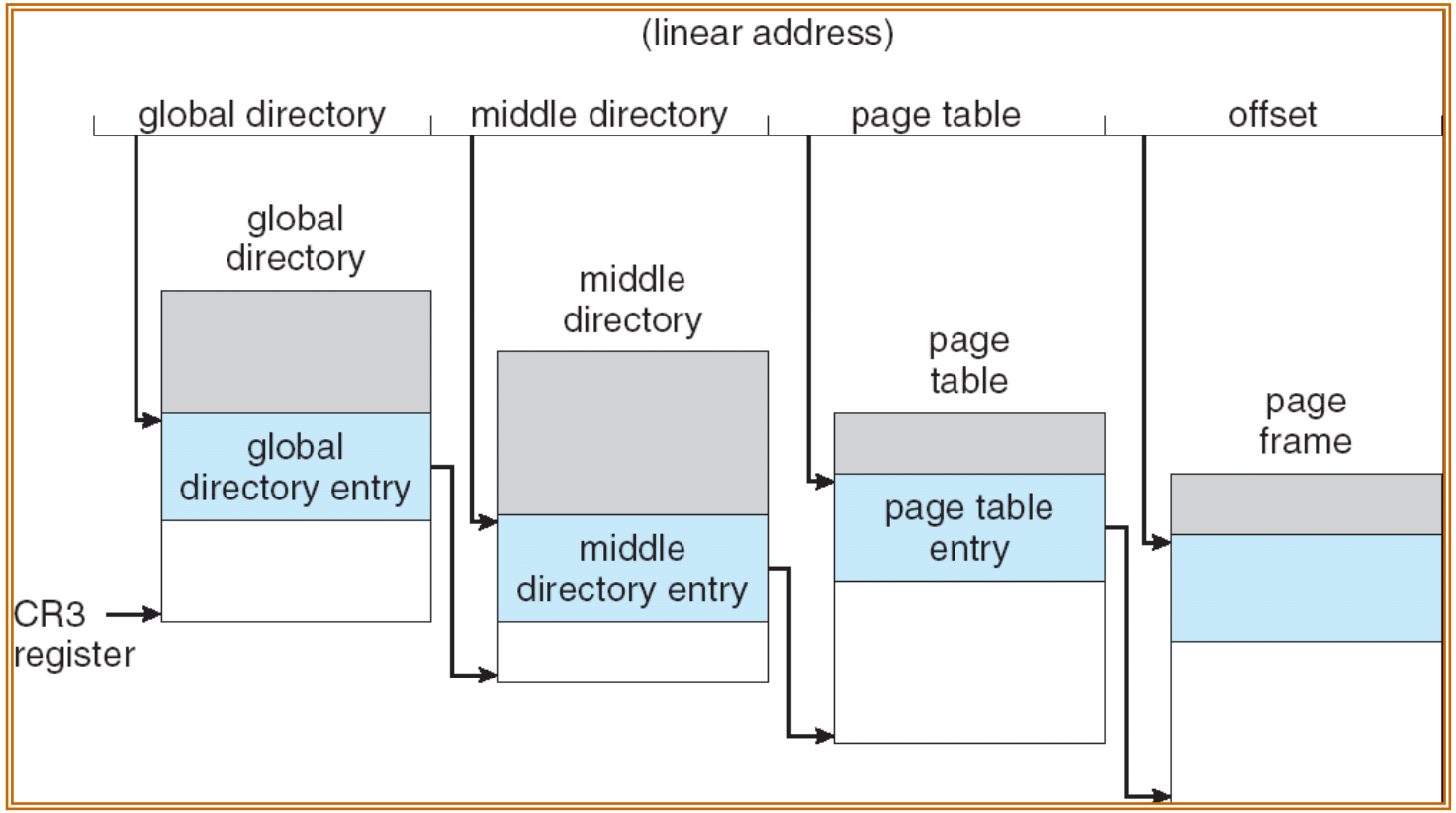
Three-level Paging in Linux (non-x86_64)



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